

Camosun College Computer Science Department

COMP182 Final Examination

23 March, 2004

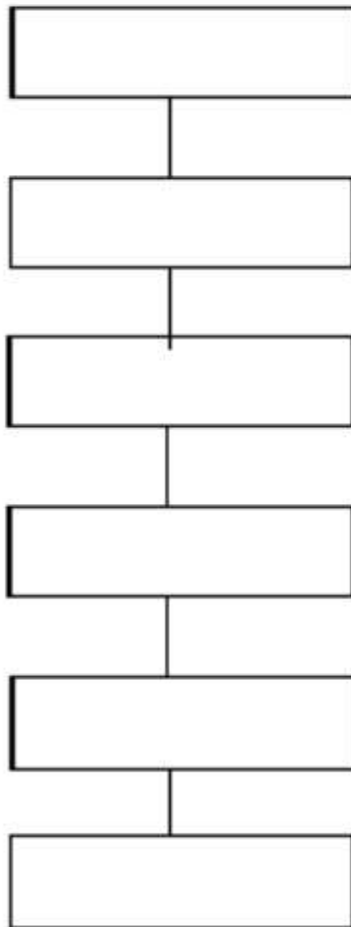
Time allowed: 2 hours

Answer *all* questions. If you do not understand something in a question, ask for help. If you do not have enough room, you may write on the back of the paper. There are 6 pages, including this one.

Name: _____

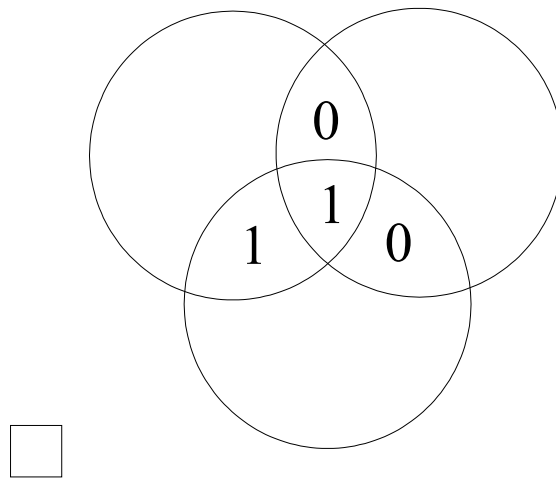
Marks/75 _____ (Do *not* fill this in)

1. Fill in the names of the six levels in the virtual machine hierarchy. Describe briefly how each level is supported by the one(s) below it. (9 marks)

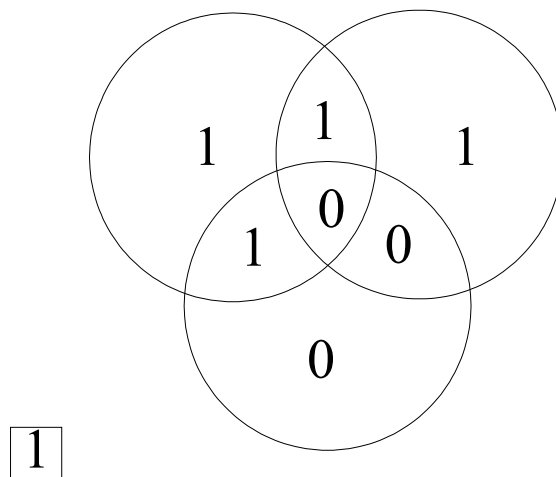


2. EDAC SEC-DED

- i. Fill in the parity bits in the following diagram for an *even* parity scheme (2 marks).



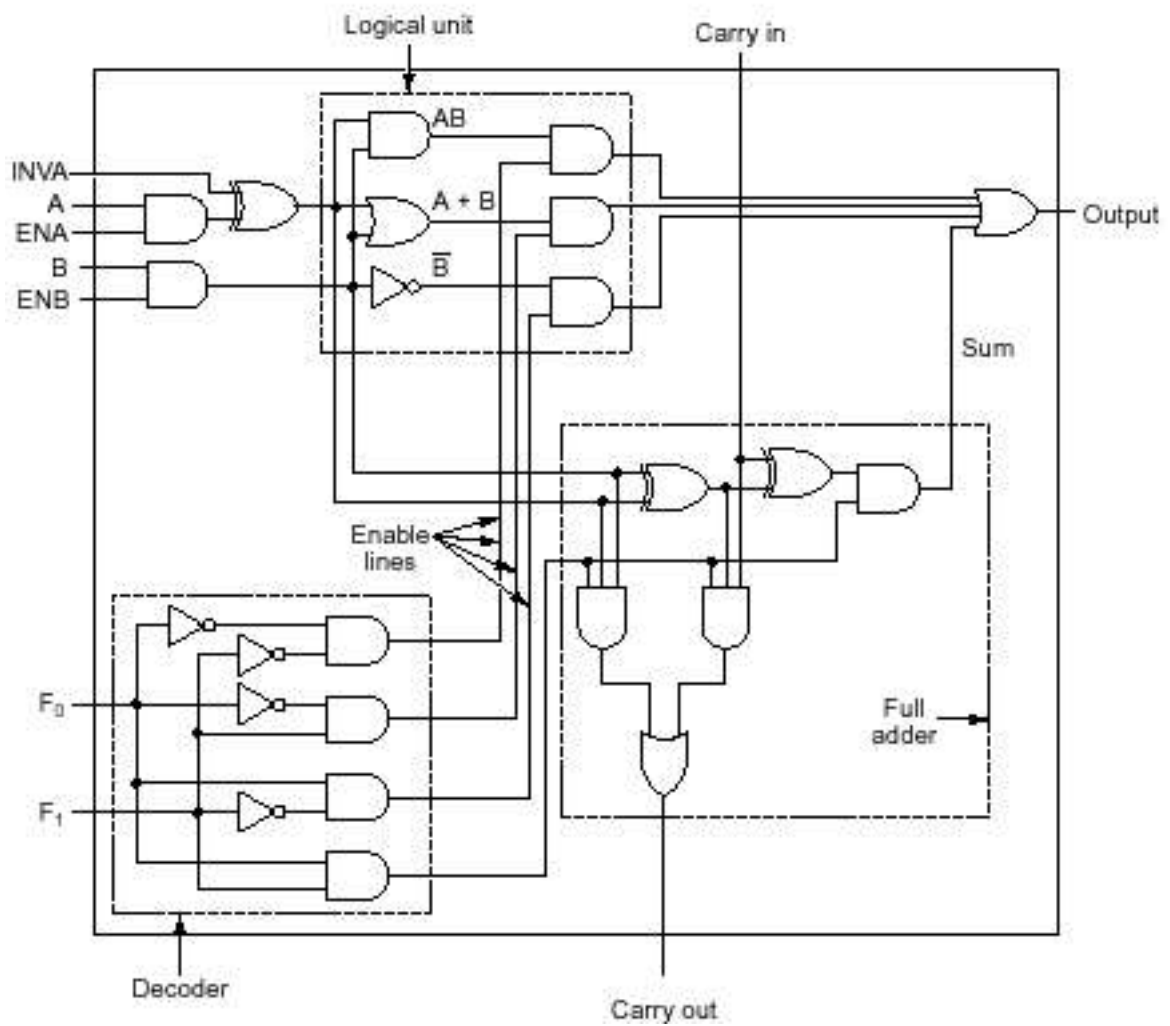
- ii. The following diagram (also *even* parity) is shown *after transmission*. Show which bit has apparently been altered and say whether or not the error is recoverable. Do *not* assume that this diagram is derived from the previous one. (3 marks).



4. State six things which are carried out at *interrupt time*. Specify which are done by the hardware and which are done by software in the ISR. (12 marks)

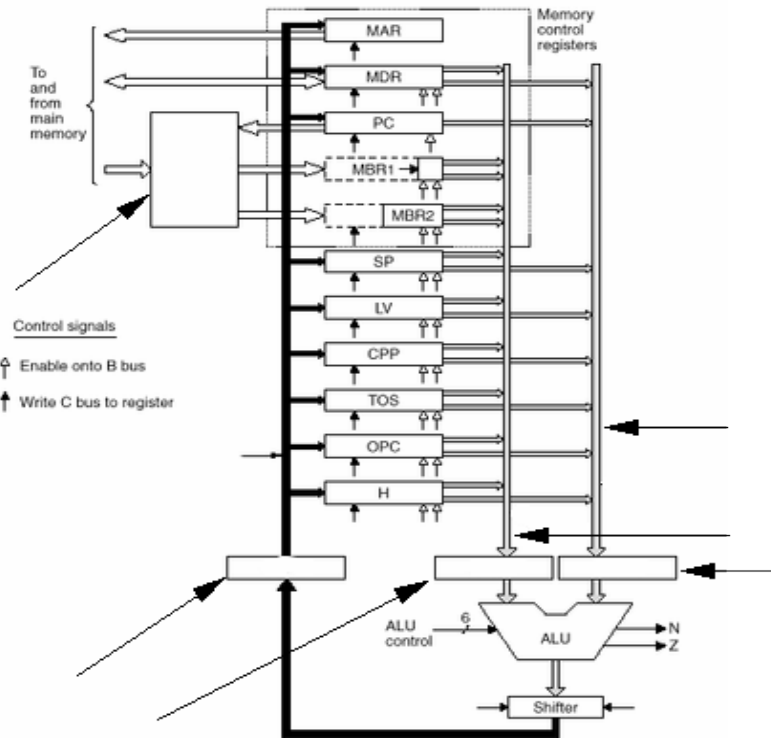
6. Often when a chip manufacturer brings out a new version of a particular CPU the pipeline is made longer. Why is this done? What problems can it cause? (9 marks)

5. The following circuit diagram shows a 1-bit ALU. State, in terms of the inputs A and B, what function the ALU will output for each combination of control signals specified below. (*INC* means the Carry In line). (10 marks)



F_0	F_1	ENA	ENB	INVA	INC	Function
1	1	1	1	1	1	
1	1	0	1	0	1	
0	0	1	1	0	0	
1	1	1	1	0	0	
0	1	0	1	0	0	

6. The following diagram shows the data path of a sample architecture. (10 marks total)



- i. Indicate the pipeline stages in the data path and state their usual names
- ii. Show how, by writing under the column headers provided, you would achieve the following two functions on the architecture. For each micro-operation state a) the registers to be loaded onto the input buses b) the ALU and shifter functions c) which register(s) should be stored into from the output bus d) any memory control lines (e.g. read) which need to be asserted.

Notes: the ALU is capable of at least the following functions (A is left input, B is right input): A, B, not A, not B, A OR B, A AND B, A + B, A + 1, B + 1, A + B + 1, B - 1, B - A. The shifter can shift 1 bit left (L), right (R) or not at all (N). The TOS register keeps a copy of the Top Of Stack and *must* be kept current.

1. Multiply the H register by 2

REGS to BUSES A, B ALU, SHIFTER C BUS to REG(s) MEMORY

2. Push CPP + 1 onto the stack

REGS to BUSES A, B ALU, SHIFTER C BUS to REG(s) MEMORY

7. Name the three major cache memory organisations. briefly describe how one of them works. State its advantages and disadvantages. (10 marks)

8. Why does branch prediction help keep a pipeline moving? Draw the state transition diagram for the 2-bit Branch History Table ("I'll give you one more chance") Entry, labelling the transitions. Give an example of the kind of level 2 (machine) code this model is specifically designed to deal with. (10 marks)